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# PATENT ABSTRACTS OF JAPAN

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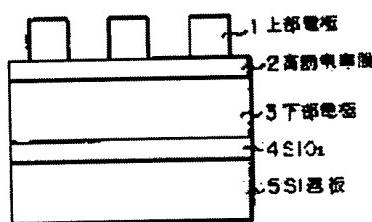
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## **(54) THIN FILM CAPACITOR, ITS MANUFACTURE AND WORKING METHOD OF ELECTRODE**

(57)Abstract:

PROBLEM TO BE SOLVED: To realize a thin film capacitor wherein leak current density is small, by forming a first electrode layer which is in contact with at least a high permittivity film of an upper electrode film and has a specified thickness, of ruthenium or ruthenium oxide.

SOLUTION: In a thin film capacitor, BST is used as a high permittivity film 2, and a silicon (Si) substrate 5 has a surface which is SiO<sub>2</sub> 4 formed by heat treatment, on which substrate 5 the following are formed; Pt as a lower electrode 3, a high permittivity film 2, and single layer Ru as upper electrodes which are 30nm in thickness. An upper electrode film 1 is composed a single layer or a plurality of layers. The first electrode layer which is in contact with at least the high permittivity film 2 is composed of ruthenium(Ru) or ruthenium oxide (RUO<sub>2</sub>). It is especially



important that the thickness of the layer is less than 50nm and greater than or equal to 5nm. Thereby a thin film capacitor excellent in electric characteristics can be realized.

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#### CLAIMS

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##### [Claim(s)]

[Claim 1] The thin film capacitor characterized by for the 1st electrode layer of this up electrode layer which touches this high dielectric constant film at least being a ruthenium (Ru) or ruthenium oxide (RuO<sub>2</sub>), and the thickness of the aforementioned electrode layer being less than 50nm in the thin film capacitor of the structure inserted by the up electrode layer which a high dielectric constant thin film turns into from a lower electrode layer and a monolayer, or two or more layers.

[Claim 2] The manufacture method of the thin film capacitor of the structure inserted by the up electrode layer which is characterized by providing the following, and which a high dielectric constant thin film turns into from a lower electrode layer and a monolayer, or two or more layers The process which forms a ruthenium (Ru) or ruthenium oxide (RuO<sub>2</sub>) as an electrode layer of this up electrode thin film which touches this high

dielectric constant film at least As 2nd electrode layer which is the best layer of this up electrode thin film, it is oxygen.

[Claim 3] The electrode layer of the above 2nd is the manufacture method of the thin film capacitor according to claim 2 which is either aluminum (aluminum), titanium (Ti) or a titanium nitride (TiN).

[Claim 4] A high dielectric constant film is the manufacture method of the thin film capacitor of the structure inserted by the lower electrode and the up electrode. In the manufacture method by which the process of the dry etching in the atmosphere which contains the oxygen of a ruthenium (Ru) or a ruthenium oxide (RuO<sub>2</sub>) layer in a lower electrode or an up electrode at least is included The manufacture method of the thin film capacitor characterized by a dry dirty process being an etching process in the electrode structure where the maximum front face of this electrode was formed by either aluminum (aluminum), titanium (Ti) or the titanium nitride (TiN) in the electrode layer of this ruthenium or ruthenium oxide.

[Claim 5] It is the electrode which consisted of a monolayer or two or more layers. to the aforementioned electrode A ruthenium (Ru), Or it sets to the processing method of an electrode of having a dry etching process in the atmosphere in which the layer of ruthenium oxide (RuO<sub>2</sub>) is contained in, and this ruthenium (Ru) or this ruthenium oxide (RuO<sub>2</sub>) contains oxygen. The processing method of the electrode characterized by the process of the aforementioned dry etching being an etching process in the electrode structure where the maximum front face of this electrode was formed by either aluminum (aluminum), titanium (Ti) or the titanium nitride (TiN).

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## DETAILED DESCRIPTION

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### [Detailed Description of the Invention]

#### [0001]

[The technical field to which invention belongs] this invention relates to the object for semiconductor devices, and the thin film capacitor for integrated circuits especially about a thin film capacitor, its manufacture method, and the processing method of an electrode.

#### [0002]

[Description of the Prior Art] SrTiO<sub>3</sub> which was excellent in dielectric characteristics, insulation, and chemical stability in order to apply to the capacity film for next-generation high-density DRAM of 1 or more Gbits, TiO<sub>x</sub>(Ba, Sr)<sub>3</sub> (henceforth BST), and TiO<sub>x</sub>(Pb, Zr)<sub>3</sub> etc. -- research and development of a perovskite type oxide dielectric thin film are done Simultaneously, in order to depend in the electrode material and process

strongly, examination of an electrode material is also important for the electrical property of a dielectric thin film.

[0003] Ru or RuO<sub>2</sub> It has the feature that the processability is good, and the application as an electrode material of a BST film is considered. About the thin film capacitor using Ru as an electrode material, and its manufacture method, A. YUUKI etc. is reported in detail to a technical digest, 115-118 pages and this technical digest, and 903-906 pages by Y. rock shell ochre etc. in International electron device "meeting IEDM"" 1995, respectively.

[0004] The publication of the thickness of Ru does not have an up electrode in the thin film capacitor using Ru monolayer, using barium-titanate strontium (Ba, Sr) (it omitting below TiO<sub>3</sub>; BST) as a conventional high dielectric constant film. Moreover, by the manufacture method of the conventional thin film capacitor, micro processing of Ru is SiO<sub>2</sub>. It is carried out by the reactive-ion-etching method using the mask.

[0005]

[Problem(s) to be Solved by the Invention] Generally, in order to make the capacity of a thin film capacitor increase, it is required to make thin thickness of the high dielectric constant film which is an electrode spacing, i.e., a capacity film. When next-generation high-density DRAM of 1 or more Gbits is considered especially, even if it uses high dielectric constant films, such as BST, about 20-30nm needs to be ultra-thin-film-ized. However, ultra-thin film-ization of such a high dielectric constant film has the problem of increasing the leakage current of a thin film capacitor. Generally, the area of a capacitor is taken into consideration, it is such leakage-current density of a thin film capacitor at the 1V impression time, and less than [ 1x10<sup>-8</sup>Acm<sup>-2</sup> ] is needed.

[0006] In the conventional thin film capacitor, when the thickness of BST was 25nm, the leakage-current density in the time of 1V impression is abbreviation 4x10<sup>-8</sup>Acm<sup>-2</sup>, and had the problem that the current density demanded was not reached.

[0007] On the other hand, it is SiO<sub>2</sub> on Ru electrode in the case of processing of the up electrode Ru by the manufacture method of the conventional thin film capacitor. Membranes are formed, a resist is processed with the photolithography technology which applies a resist and is generally used, and it is SiO<sub>2</sub>. Patterning was carried out and Ru was processed. Thus, at a Prior art, it is SiO<sub>2</sub>. The process of membrane formation and removal entered and there was a problem in respect of a throughput.

[0008] Moreover, it is SiO<sub>2</sub> although Ru must be processed in 0.1-0.2-micron size in case Ru is used for the lower electrode of next-generation high-density DRAM of 1 or more Gbits. When a mask was used, while there was a problem in respect of a throughput by the above-mentioned reason, the problem was in the processing configuration. This is SiO<sub>2</sub>. It is amorphous and is SiO<sub>2</sub> to Ru dry etching. By a shoulder \*\*\*\*\*ing, it is SiO<sub>2</sub>. For mask area to become small and it is hard to process processed Ru perpendicularly.

[0009] The purpose of this invention is to offer a thin film capacitor with small leakage-current density. Moreover, a throughput is high, and since it is a process in low temperature, it is in offering the manufacture method of a thin film capacitor of not degrading the circuit property of a semiconductor, and it is in offering the manufacture method of the thin film capacitor which processing of further super-large scale integration can attain in the target processing configuration, and the processing method of an electrode.

[0010]

[Means for Solving the Problem] The aforementioned purpose is attained by the following meanses. That is, this invention proposes the thin film capacitor characterized by for the 1st electrode layer of this up electrode layer which touches this high dielectric constant film at least being a ruthenium (Ru) or ruthenium oxide (RuO<sub>2</sub>), and the thickness of the aforementioned electrode layer being less than 50nm in the thin film capacitor of the structure inserted by the up electrode layer which a high dielectric constant thin film turns into from a lower electrode layer and a monolayer, or two or more layers.

[0011] Moreover, a high dielectric constant thin film sets this invention to the manufacture method of the thin film capacitor of the structure inserted by the up electrode layer which consists of a lower electrode layer and a monolayer, or two or more layers. The process which forms a ruthenium (Ru) or ruthenium oxide (RuO<sub>2</sub>) as an electrode layer of this up electrode thin film which touches this high dielectric constant film at least, [ whether as 2nd electrode layer which is the best layer of this up electrode thin film, the dry etching in the atmosphere containing oxygen \*\*\*\*\*'s, and ] Or it is what proposes the manufacture method of the thin film capacitor characterized by including at least the process which forms the conductive electrode material whose etch rate of dry etching is 1/10 or less [ of the etch rate of the 1st electrode layer ]. It includes that the electrode layer of the above 2nd is either aluminum (aluminum), titanium (Ti) or a titanium nitride (TiN).

[0012] Moreover, this invention is the manufacture method of the thin film capacitor of the structure where the high dielectric constant film was inserted by the lower electrode and the up electrode. In the manufacture method by which the process of the dry etching in the atmosphere which contains the oxygen of a ruthenium (Ru) or a ruthenium oxide (RuO<sub>2</sub>) layer in a lower electrode or an up electrode at least is included The electrode layer of this ruthenium or ruthenium oxide a dry dirty process It is what proposes the manufacture method of the thin film capacitor characterized by being an etching process in the electrode structure where the maximum front face of this electrode was formed by either aluminum (aluminum), titanium (Ti) or the titanium nitride (TiN). this invention is the electrode which consisted of a monolayer or two or more layers. to the aforementioned electrode Furthermore, a ruthenium (Ru), Or it sets to the processing method of an electrode of having a dry etching process in the atmosphere in which the layer of ruthenium oxide (RuO<sub>2</sub>) is contained in, and this ruthenium (Ru) or this ruthenium oxide (RuO<sub>2</sub>) contains oxygen. The processing method of the electrode characterized by the process of the aforementioned dry etching being an etching process in the electrode structure where the maximum front face of this electrode was formed by either aluminum (aluminum), titanium (Ti) or the titanium nitride (TiN) is proposed.

[0013]

[Embodiments of the Invention] Hereafter, this invention is explained still in detail.

[0014] this invention person etc. uses BST as a high dielectric constant film, and is Ru and RuO<sub>2</sub> as an up electrode. It used, respectively, the thin film capacitor was formed, and the leakage-current property was investigated. A lower electrode is platinum (Pt). Consequently, it found out that a leakage current decreased by setting thickness of an up electrode to 100nm or less. Simultaneously, thickness found out that the downward tendency of a leakage current was remarkable by less than 50nm. When thickness of an

up electrode was based on 200nm, thickness decreased to 10 by about 1/by 50nm, and thickness decreased to 15 by about 1/in 30nm. Although the detail of this reason is unknown, reduction of the damage to the BST film at the time of up electrode formation and reduction of stress can be considered.

[0015] this invention person etc. is Ru and RuO<sub>2</sub> as an up electrode layer which touches BST, using BST as a high dielectric constant film. aluminum, Ti, and TiN were formed in the upper part, respectively. It is Ru and RuO<sub>2</sub>, applying a resist besides, processing a resist with the usual photolithography technology, and using it as a mask. Dry etching of each upper conductive electrode was carried out. Chlorine gas was used at this time. Continuously, it is Ru and RuO<sub>2</sub> in the atmosphere containing oxygen. When dry etching is carried out, it is Ru and RuO<sub>2</sub>. Although etching advances with etching also in a resist, it is Ru and RuO<sub>2</sub>. The upper conductive electrode is not made to \*\*\*\*\* but is Ru and RuO<sub>2</sub>. It turns out that it is processible. The resist which remained is O<sub>2</sub>. It was easily removable by ashing. Simultaneously, it is Ru and RuO<sub>2</sub>. When the upper conductive electrode was usable as an up electrode as it is and it was unnecessary, the thing possible dirtily in a businesslike manner was also continuously checked after resist removal. At this technique, it is SiO<sub>2</sub>. It became clear that the process of formation and removal is unnecessary, it is very simple, and a throughput is high. Moreover, it is Ru of the 1st electrode, and RuO<sub>2</sub>, without making the 2nd electrode \*\*\*\*\* even if the etch rate of dry etching uses 1/10 or less electrode material of the etch rate of the 1st electrode layer as 2nd electrode layer. It turns out that it is processible.

[0016] the same -- especially -- Ru and RuO<sub>2</sub> the time of it being overly detailed-alike and processing it -- Ru and RuO<sub>2</sub> Although aluminum, Ti, or TiN was formed in the upper surface of an electrode and dry etching processing was performed at the same process as the above, it was possible to have not carried out the shoulder collapse of aluminum, Ti, or the TiN at all, but to have processed Ru and RuO<sub>2</sub> into a perpendicular mostly.

[0017] Furthermore, this invention is explained with reference to a drawing.

[0018] Drawing 1 is the cross section showing an example of the thin film capacitor of this invention. The thin film capacitor of this invention comes to prepare the structure where the high dielectric constant thin film 2 was inserted by the lower electrode 3 and the up electrode layer 1 on the SiO<sub>2</sub> silicon (Si) substrate 5 in which the substrate front face was formed by thermal oxidation and which has 4, as shown in drawing 1.

[0019] as the high dielectric constant thin film 2 -- SrTiO<sub>3</sub>, TiO<sub>3</sub> (Ba, Sr)3 (BST), BaTiO<sub>3</sub>, TiO<sub>3</sub> (Pb, Zr)3, and SrBi<sub>2</sub> Ta 2O<sub>9</sub> etc. -- it is mentioned and the range of thickness of 15-200nm is desirable

[0020] It consists of a monolayer or two or more layers, and the 1st electrode layer which touches a high dielectric constant film at least consists of a ruthenium (Ru) or ruthenium oxide (RuO<sub>2</sub>), and, as for the up electrode layer 1, it is important that the thickness is especially less than 50nm 5nm or more.

[0021] Since the leakage current of a thin film capacitor will be increased if thickness exceeds 50nm, it is [ a problem (local discontinuity in a field) from which a homogeneous membrane is hard to be obtained in less than 5nm ] preferably and is not desirable. Moreover, when the up electrode layer 1 consists of two or more layers, as the 2nd electrode layer, aluminum (aluminum), titanium (Ti), or a titanium nitride (TiN) is used preferably.

[0022] Moreover, Pt, Ru, RuO<sub>2</sub>, Ir, and IrO<sub>2</sub> grade are mentioned as a lower electrode 3, and the range of thickness of 5-500nm is desirable.

[0023] Each aforementioned film can be formed by methods, such as the DC magnetron-sputtering method, the RF magnetron-sputtering method, an efficient consumer response spatter, and a vapor growth.

[0024]

[Example] An example explains this invention still more concretely below.

[0025] (Example 1) The example of this invention is explained hereafter, referring to drawing 1. Drawing 1 is the cross section of the thin film capacitor in connection with an example 1. It has the structure where 30nm of Ru of a monolayer was formed as Pt, the high dielectric constant film 2, and an up electrode as a lower electrode 3 on the SiO<sub>2</sub> silicon (Si) substrate 5 in which the substrate front face was formed by thermal oxidation and which has 4, using BST as a high dielectric constant film 2. In this example, BST thickness is 30nm and all the films were formed by the DC magnetron sputtering method. The configuration of an up electrode is the round shape of 0.2mmphi. As a result of measuring an electrical property, the dielectric constant was 290 and the leakage-current density J was  $8 \times 10^{-9} \text{ Acm}^{-2}$ . In order to investigate the effect of thin-film-izing of Ru of this invention, as a result of changing the thickness of Ru which is an up electrode to 200nm and investigating it to the same sample, by 200nm, J is  $1.5 \times 10^{-8} \text{ Acm}^{-2}$  in  $8 \times 10^{-8} \text{ Acm}^{-2}$ , 100nm, and the effect which is this invention was checked. The dielectric constant bases on the thickness of an up electrode and was fixed.

[0026] (Example 2) It has structure which is the electrode by which Ru (30nm) and aluminum (100nm) were carried out as a lower electrode 3 like the example 1 on the SiO<sub>2</sub> silicon (Si) substrate 5 in which the substrate front face was formed by thermal oxidation, and which has 4, using BST as a high dielectric constant film 2, and the laminating was carried out to the order of a lower shell as Pt, the high dielectric constant film 2, and an up electrode. In this example, BST thickness is 30nm and all the films were formed by the DC magnetron sputtering method. The configuration of an up electrode is the round shape of 0.2mmphi. As a result of measuring an electrical property, the dielectric constant was 290 and the leakage-current density J was  $8 \times 10^{-9} \text{ Acm}^{-2}$ . In order to investigate the effect of this invention, the same with having carried out in the example 1, the thickness of aluminum of an up electrode layer was set constant, and the effect of thin-film-izing of Ru was investigated. It is completely the same as that of an example 1, and a result is a book.

[0027] (Example 3) By this example, the example which used TiN as Ru and 2nd electrode layer as 1st electrode layer of BST and the up electrode 1 as RuO<sub>2</sub> and a high dielectric constant film 2 as a lower electrode 3 is explained, referring to drawing 2.

[0028] On the SiO<sub>2</sub> silicon (Si) substrate 5 which was formed by thermal oxidation and which has 4, the substrate front face formed the lower electrode 3 (RuO<sub>2</sub>), the high dielectric constant film 2 (BST), the 1st electrode layer 6 of the up electrode 1 (Ru), and the 2nd electrode layer 7 (TiN) by the DC magnetron-sputtering method one by one. 30nm and the 2nd electrode layer set thickness to 200nm, and 30nm and the 1st electrode layer set [the lower electrode] BST to 70nm. Continuously, the resist 8 was applied and the substrate shown in drawing 2 (a) was obtained. With the lithography technology by the usual i line, it exposed, the resist was processed, and drawing 2 (b) was formed. It is TiN which this substrate is put into a dry etching system, and is the 2nd electrode layer 7

first Cl2 It \*\*\*\*\*ed by plasma gas. At this time, the chamber pressures of an etching system were 15mTorr(s), and plasma power was 50W. Ru which is the 1st electrode layer 6 continuously -- O<sub>2</sub> Cl2 mixed gas (Cl2 is 10%) -- using -- etching -- the bottom The chamber pressures at this time are 20mTorr(s), and plasma power is 100W. Although most resists disappeared Ru in dry etching, in order to remove the resist which remained, ashing by oxygen plasma removed. Consequently, the thin film capacitor into which the up electrode as shown in drawing 2 (c) was processed was obtained. Similarly, although inquired by the same manufacture method, using aluminum or Ti as 2nd electrode layer, the completely same thin film capacitor was obtained. The electrical property of this capacitor showed the same good property as examples 1 and 2.

[0029] At this process, it is SiO<sub>2</sub> as a mask. It does not form but is a book.

[0030] Cl2 although the 2nd electrode layer was not removed but it was used as it is as an electrode in the above-mentioned example, after carrying out ashing removal of the resist. Although the thin film capacitor from which the 2nd electrode layer 7 (TiN) was removed by the dry etching by plasma gas was also made, the case where it does not remove, and the electrical property were the same.

[0031] (Example 4) this example explains Ru which is a lower electrode using drawing 3 about the example which carried out micro processing very much.

[0032] On the SiO<sub>2</sub> silicon (Si) substrate 5 in which the substrate front face was formed by thermal oxidation and which has 4, Ru9 was formed by 300nm and TiN10 was formed by 100nm and the DC magnetron-sputtering method. The substrate which drawing 3 (a) Comes to apply the chemistry amplification resist 8 to this substrate was formed. By electron beam exposure, the processing size 0.2 micron x0.5 micron pattern was formed, and the substrate which drawing 3 (b) Comes to process a resist 8 was formed. It is Cl2 about TiN10, putting this substrate into a dry etching system, and using a resist 8 as a mask. Etching by plasma was performed. The pressures of the etching system at this time are 15mTorr(s), and plasma power is 50W. continuing -- Ru 9O<sub>2</sub> Cl2 mixed gas (Cl2 is 10%) -- using -- etching -- the bottom The chamber pressures at this time are 20mTorr(s), and plasma power is 100W. The resist disappeared Ru in dry etching. Continuously, it is Cl2 about TiN10. Plasma etching was carried out, it removed and the substrate shown in drawing 3 (c) was obtained. The pressures of the etching system at this time are 15mTorr(s), and plasma power is 50W.

[0033] As a result of observing the obtained substrate with an electron microscope, it checked that processing was made as a design size. Moreover, the same result was obtained although experimented also about the case where Ti or aluminum is used for a change of TiN.

[0034] in the above-mentioned example, although BST was used as a high dielectric constant film, this invention is limited to this material -- not having -- a strontium titanate (SrTiO<sub>3</sub>), a barium titanate (BaTiO<sub>3</sub>), and TiO(Pb, Zr) 3 SrBi<sub>2</sub> Ta 2O<sub>9</sub> etc. -- other high dielectric films are sufficient

[0035] Although the DC magnetron-sputtering method was used as the membrane formation method of an electrode and a dielectric in the above-mentioned example, this invention may not be limited to this but the RF magnetron-sputtering method, an efficient consumer response sputter, and \*\*\*\*\* are sufficient as it.

[0036] Although Ru was used in the above-mentioned example, this invention may not be limited to this material, but RuO<sub>2</sub> is sufficient as it.

[0037]

[Effect of the Invention] As mentioned above, as explained, according to the thin film capacitor of this invention, it is effective in leakage-current density being small and excelling in an electrical property. Moreover, according to the manufacture method of the thin film capacitor of this invention, a throughput is high, and since it is a process in low temperature, it is effective in the ability of processing of further super-large scale integration which does not degrade the circuit property of a semiconductor to attain in the target processing configuration.

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[Translation done.]

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## TECHNICAL FIELD

---

[The technical field to which invention belongs] this invention relates to the object for semiconductor devices, and the thin film capacitor for integrated circuits especially about a thin film capacitor, its manufacture method, and the processing method of an electrode.

[0002]

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[Translation done.]

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## PRIOR ART

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[Description of the Prior Art] SrTiO<sub>3</sub> which was excellent in dielectric characteristics, insulation, and chemical stability in order to apply to the capacity film for next-generation high-density DRAM of 1 or more Gbits, TiO<sub>3</sub> (Ba, Sr)<sub>3</sub> (henceforth BST), and TiO<sub>3</sub> (Pb, Zr)<sub>3</sub> etc. -- research and development of a perovskite type oxide dielectric thin film are done Simultaneously, in order to depend in the electrode material and process strongly, examination of an electrode material is also important for the electrical property of a dielectric thin film.

[0003] Ru or RuO<sub>2</sub> It has the feature that the processability is good, and the application as an electrode material of a BST film is considered. About the thin film capacitor using Ru as an electrode material, and its manufacture method, A. YUUKI etc. is reported in detail to a technical digest, 115-118 pages and this technical digest, and 903-906 pages by Y. rock shell ochre etc. in International electron device "meeting IEDM"" 1995, respectively.

[0004] The publication of the thickness of Ru does not have an up electrode in the thin film capacitor using Ru monolayer, using barium-titanate strontium (Ba, Sr) (it omitting below TiO<sub>3</sub>; BST) as a conventional high dielectric constant film. Moreover, by the manufacture method of the conventional thin film capacitor, micro processing of Ru is SiO<sub>2</sub>. It is carried out by the reactive-ion-etching method using the mask.

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[Translation done.]

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## EFFECT OF THE INVENTION

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[Effect of the Invention] As mentioned above, as explained, according to the thin film capacitor of this invention, it is effective in leakage-current density being small and excelling in an electrical property. Moreover, according to the manufacture method of the thin film capacitor of this invention, a throughput is high, and since it is a process in low temperature, it is effective in the ability of processing of further super-large scale integration which does not degrade the circuit property of a semiconductor to attain in the target processing configuration.

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## TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Generally, in order to make the capacity of a thin film capacitor increase, it is required to make thin thickness of the high dielectric constant film which is an electrode spacing, i.e., a capacity film. When next-generation high-density DRAM of 1 or more Gbits is considered especially, even if it uses high dielectric constant films, such as BST, about 20-30nm needs to be ultra-thin-film-ized. However, ultra-thin film-ization of such a high dielectric constant film has the problem of increasing the leakage current of a thin film capacitor. Generally, the area of a capacitor is taken into consideration, it is such leakage-current density of a thin film capacitor at the 1V impression time, and less than [ 1x10<sup>-8</sup>Acm<sup>-2</sup> ] is needed.

[0006] In the conventional thin film capacitor, when the thickness of BST was 25nm, the leakage-current density in the time of 1V impression is abbreviation 4x10<sup>-8</sup>Acm<sup>-2</sup>, and had the problem that the current density demanded was not reached.

[0007] On the other hand, it is SiO<sub>2</sub> on Ru electrode in the case of processing of the up electrode Ru by the manufacture method of the conventional thin film capacitor.

Membranes are formed, a resist is processed with the photolithography technology which applies a resist and is generally used, and it is SiO<sub>2</sub>. Patterning was carried out and Ru was processed. Thus, at a Prior art, it is SiO<sub>2</sub>. The process of membrane formation and removal entered and there was a problem in respect of a throughput.

[0008] Moreover, it is SiO<sub>2</sub> although Ru must be processed in 0.1-0.2-micron size in case Ru is used for the lower electrode of next-generation high-density DRAM of 1 or more Gbits. When a mask was used, while there was a problem in respect of a throughput by the above-mentioned reason, the problem was in the processing configuration. This is SiO<sub>2</sub>. It is amorphous and is SiO<sub>2</sub> to Ru dry etching. By a shoulder \*\*\*\*\*ing, it is SiO<sub>2</sub>. For mask area to become small and it is hard to process processed Ru perpendicularly.

[0009] The purpose of this invention is to offer a thin film capacitor with small leakage-

current density. Moreover, a throughput is high, and since it is a process in low temperature, it is in offering the manufacture method of a thin film capacitor of not degrading the circuit property of a semiconductor, and it is in offering the manufacture method of the thin film capacitor which processing of further super-large scale integration can attain in the target processing configuration, and the processing method of an electrode.

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[Translation done.]

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## MEANS

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[Means for Solving the Problem] The aforementioned purpose is attained by the following meanses. That is, this invention proposes the thin film capacitor characterized by for the 1st electrode layer of this up electrode layer which touches this high dielectric constant film at least being a ruthenium (Ru) or ruthenium oxide (RuO<sub>2</sub>), and the thickness of the aforementioned electrode layer being less than 50nm in the thin film capacitor of the structure inserted by the up electrode layer which a high dielectric constant thin film turns into from a lower electrode layer and a monolayer, or two or more layers.

[0011] Moreover, a high dielectric constant thin film sets this invention to the manufacture method of the thin film capacitor of the structure inserted by the up electrode layer which consists of a lower electrode layer and a monolayer, or two or more layers. The process which forms a ruthenium (Ru) or ruthenium oxide (RuO<sub>2</sub>) as an electrode layer of this up electrode thin film which touches this high dielectric constant film at least, [ whether as 2nd electrode layer which is the best layer of this up electrode thin film, the dry etching in the atmosphere containing oxygen \*\*\*\*\*'s, and ] Or it is what proposes the manufacture method of the thin film capacitor characterized by including at least the process which forms the conductive electrode material whose etch rate of dry etching is 1/10 or less [ of the etch rate of the 1st electrode layer ]. It includes that the electrode layer of the above 2nd is either aluminum (aluminum), titanium (Ti) or a titanium nitride (TiN).

[0012] Moreover, this invention is the manufacture method of the thin film capacitor of the structure where the high dielectric constant film was inserted by the lower electrode and the up electrode. In the manufacture method by which the process of the dry etching in the atmosphere which contains the oxygen of a ruthenium (Ru) or a ruthenium oxide (RuO<sub>2</sub>) layer in a lower electrode or an up electrode at least is included The electrode layer of this ruthenium or ruthenium oxide a dry dirty process It is what proposes the manufacture method of the thin film capacitor characterized by being an etching process in the electrode structure where the maximum front face of this electrode was formed by either aluminum (aluminum), titanium (Ti) or the titanium nitride (TiN). this invention is the electrode which consisted of a monolayer or two or more layers. to the aforementioned electrode Furthermore, a ruthenium (Ru), Or it sets to the processing method of an electrode of having a dry etching process in the atmosphere in which the layer of ruthenium oxide (RuO<sub>2</sub>) is contained in, and this ruthenium (Ru) or this

ruthenium oxide (RuO<sub>2</sub>) contains oxygen. The processing method of the electrode characterized by the process of the aforementioned dry etching being an etching process in the electrode structure where the maximum front face of this electrode was formed by either aluminum (aluminum), titanium (Ti) or the titanium nitride (TiN) is proposed.

[0013]

[Embodiments of the Invention] Hereafter, this invention is explained still in detail.

[0014] this invention person etc. uses BST as a high dielectric constant film, and is Ru and RuO<sub>2</sub> as an up electrode. It used, respectively, the thin film capacitor was formed, and the leakage-current property was investigated. A lower electrode is platinum (Pt). Consequently, it found out that a leakage current decreased by setting thickness of an up electrode to 100nm or less. Simultaneously, thickness found out that the downward tendency of a leakage current was remarkable by less than 50nm. When thickness of an up electrode was based on 200nm, thickness decreased to 10 by about 1/by 50nm, and thickness decreased to 15 by about 1/in 30nm. Although the detail of this reason is unknown, reduction of the damage to the BST film at the time of up electrode formation and reduction of stress can be considered.

[0015] this invention person etc. is Ru and RuO<sub>2</sub> as an up electrode layer which touches BST, using BST as a high dielectric constant film. aluminum, Ti, and TiN were formed in the upper part, respectively. It is Ru and RuO<sub>2</sub>, applying a resist besides, processing a resist with the usual photolithography technology, and using it as a mask. Dry etching of each upper conductive electrode was carried out. Chlorine gas was used at this time.

Continuously, it is Ru and RuO<sub>2</sub> in the atmosphere containing oxygen. When dry etching is carried out, it is Ru and RuO<sub>2</sub>. Although etching advances with etching also in a resist, it is Ru and RuO<sub>2</sub>. The upper conductive electrode is not made to \*\*\*\*\* but is Ru and RuO<sub>2</sub>. It turns out that it is processible. The resist which remained is O<sub>2</sub>. It was easily removable by ashing. Simultaneously, it is Ru and RuO<sub>2</sub>. When the upper conductive electrode was usable as an up electrode as it is and it was unnecessary, the thing possible dirtily in a businesslike manner was also continuously checked after resist removal. At this technique, it is SiO<sub>2</sub>. It became clear that the process of formation and removal is unnecessary, it is very simple, and a throughput is high. Moreover, it is Ru of the 1st electrode, and RuO<sub>2</sub>, without making the 2nd electrode \*\*\*\*\* even if the etch rate of dry etching uses 1/10 or less electrode material of the etch rate of the 1st electrode layer as 2nd electrode layer. It turns out that it is processible.

[0016] the same -- especially -- Ru and RuO<sub>2</sub> the time of it being overly detailed-alike and processing it -- Ru and RuO<sub>2</sub> Although aluminum, Ti, or TiN was formed in the upper surface of an electrode and dry etching processing was performed at the same process as the above, it was possible to have not carried out the shoulder collapse of aluminum, Ti, or the TiN at all, but to have processed Ru and RuO<sub>2</sub> into a perpendicular mostly.

[0017] Furthermore, this invention is explained with reference to a drawing.

[0018] Drawing 1 is the cross section showing an example of the thin film capacitor of this invention. The thin film capacitor of this invention comes to prepare the structure where the high dielectric constant thin film 2 was inserted by the lower electrode 3 and the up electrode layer 1 on the SiO<sub>2</sub> silicon (Si) substrate 5 in which the substrate front face was formed by thermal oxidation and which has 4, as shown in drawing 1.

[0019] as the high dielectric constant thin film 2 -- SrTiO<sub>3</sub>, TiO (Ba, Sr)3 (BST),

BaTiO<sub>3</sub>, TiO (Pb, Zr)3, and SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> etc. -- it is mentioned and the range of thickness of 15-200nm is desirable

[0020] It consists of a monolayer or two or more layers, and the 1st electrode layer which touches a high dielectric constant film at least consists of a ruthenium (Ru) or ruthenium oxide (RuO<sub>2</sub>), and, as for the up electrode layer 1, it is important that the thickness is especially less than 50nm 5nm or more.

[0021] Since the leakage current of a thin film capacitor will be increased if thickness exceeds 50nm, it is [ a problem (local discontinuity in a field) from which a homogeneous membrane is hard to be obtained in less than 5nm ] preferably and is not desirable. Moreover, when the up electrode layer 1 consists of two or more layers, as the 2nd electrode layer, aluminum (aluminum), titanium (Ti), or a titanium nitride (TiN) is used preferably.

[0022] Moreover, Pt, Ru, RuO<sub>2</sub>, Ir, and IrO<sub>2</sub> grade are mentioned as a lower electrode 3, and the range of thickness of 5-500nm is desirable.

[0023] Each aforementioned film can be formed by methods, such as the DC magnetron-sputtering method, the RF magnetron-sputtering method, an efficient consumer response sputter, and a vapor growth.

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[Translation done.]

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## EXAMPLE

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[Example] An example explains this invention still more concretely below.

[0025] (Example 1) The example of this invention is explained hereafter, referring to drawing 1 . Drawing 1 is the cross section of the thin film capacitor in connection with an example 1. It has the structure where 30nm of Ru of a monolayer was formed as Pt, the high dielectric constant film 2, and an up electrode as a lower electrode 3 on the SiO<sub>2</sub> silicon (Si) substrate 5 in which the substrate front face was formed by thermal oxidation and which has 4, using BST as a high dielectric constant film 2. In this example, BST thickness is 30nm and all the films were formed by the DC magnetron sputtering method. The configuration of an up electrode is the round shape of 0.2mmphi. As a result of measuring an electrical property, the dielectric constant was 290 and the leakage-current density J was  $8 \times 10^{-9} \text{ Acm}^{-2}$ . in order to investigate the effect of thin-film-izing of Ru of this invention, as a result of changing the thickness of Ru which is an up electrode to 200nm and investigating it to the same sample, by 200nm, J is  $1.5 \times 10^{-8} \text{ Acm}^{-2}$  in  $8 \times 10^{-8} \text{ Acm}^{-2}$ , 100nm, and the effect which is this invention was checked The dielectric constant bases on the thickness of an up electrode and was fixed.

[0026] (Example 2) It has structure which is the electrode by which Ru (30nm) and aluminum (100nm) were carried out as a lower electrode 3 like the example 1 on the SiO<sub>2</sub> silicon (Si) substrate 5 in which the substrate front face was formed by thermal oxidation, and which has 4, using BST as a high dielectric constant film 2, and the laminating was carried out to the order of a lower shell as Pt, the high dielectric constant film 2, and an up electrode. In this example, BST thickness is 30nm and all the films were formed by the DC magnetron sputtering method. The configuration of an up electrode is the round shape of 0.2mmphi. As a result of measuring an electrical property, the dielectric constant was 290 and the leakage-current density J was  $8 \times 10^{-9} \text{ Acm}^{-2}$ . In

order to investigate the effect of this invention, the same with having carried out in the example 1, the thickness of aluminum of an up electrode layer was set constant, and the effect of thin-film-izing of Ru was investigated. It is completely the same as that of an example 1, and a result is a book.

[0027] (Example 3) By this example, the example which used TiN as Ru and 2nd electrode layer as 1st electrode layer of BST and the up electrode 1 as RuO<sub>2</sub> and a high dielectric constant film 2 as a lower electrode 3 is explained, referring to drawing 2.

[0028] On the SiO<sub>2</sub> silicon (Si) substrate 5 which was formed by thermal oxidation and which has 4, the substrate front face formed the lower electrode 3 (RuO<sub>2</sub>), the high dielectric constant film 2 (BST), the 1st electrode layer 6 of the up electrode 1 (Ru), and the 2nd electrode layer 7 (TiN) by the DC magnetron-sputtering method one by one.

30nm and the 2nd electrode layer set thickness to 200nm, and 30nm and the 1st electrode layer set [ the lower electrode ] BST to 70nm. Continuously, the resist 8 was applied and the substrate shown in drawing 2 (a) was obtained. With the lithography technology by the usual i line, it exposed, the resist was processed, and drawing 2 (b) was formed. It is TiN which this substrate is put into a dry etching system, and is the 2nd electrode layer 7 first Cl<sub>2</sub> It \*\*\*\*\*ed by plasma gas. At this time, the chamber pressures of an etching system were 15mTorr(s), and plasma power was 50W. Ru which is the 1st electrode layer 6 continuously -- O<sub>2</sub> Cl<sub>2</sub> mixed gas (Cl<sub>2</sub> is 10%) -- using -- etching -- the bottom The chamber pressures at this time are 20mTorr(s), and plasma power is 100W. Although most resists disappeared Ru in dry etching, in order to remove the resist which remained, ashing by oxygen plasma removed. Consequently, the thin film capacitor into which the up electrode as shown in drawing 2 (c) was processed was obtained. Similarly, although inquired by the same manufacture method, using aluminum or Ti as 2nd electrode layer, the completely same thin film capacitor was obtained. The electrical property of this capacitor showed the same good property as examples 1 and 2.

[0029] At this process, it is SiO<sub>2</sub> as a mask. It does not form but is a book.

[0030] Cl<sub>2</sub> although the 2nd electrode layer was not removed but it was used as it is as an electrode in the above-mentioned example, after carrying out ashing removal of the resist Although the thin film capacitor from which the 2nd electrode layer 7 (TiN) was removed by the dry etching by plasma gas was also made, the case where it does not remove, and the electrical property were the same.

[0031] (Example 4) this example explains Ru which is a lower electrode using drawing 3 about the example which carried out micro processing very much.

[0032] On the SiO<sub>2</sub> silicon (Si) substrate 5 in which the substrate front face was formed by thermal oxidation and which has 4, Ru9 was formed by 300nm and TiN10 was formed by 100nm and the DC magnetron-sputtering method. The substrate which drawing 3 (a) Comes to apply the chemistry amplification resist 8 to this substrate was formed. By electron beam exposure, the processing size 0.2 micron x0.5 micron pattern was formed, and the substrate which drawing 3 (b) Comes to process a resist 8 was formed. It is Cl<sub>2</sub> about TiN10, putting this substrate into a dry etching system, and using a resist 8 as a mask. Etching by plasma was performed. The pressures of the etching system at this time are 15mTorr(s), and plasma power is 50W. continuing -- Ru 9O<sub>2</sub> Cl<sub>2</sub> mixed gas (Cl<sub>2</sub> is 10%) -- using -- etching -- the bottom The chamber pressures at this time are 20mTorr(s), and plasma power is 100W. The resist disappeared Ru in dry etching. Continuously, it is Cl<sub>2</sub> about TiN10. Plasma etching was carried out, it removed and the substrate shown in

drawing 3 (c) was obtained. The pressures of the etching system at this time are 15mTorr(s), and plasma power is 50W.

[0033] As a result of observing the obtained substrate with an electron microscope, it checked that processing was made as a design size. Moreover, the same result was obtained although experimented also about the case where Ti or aluminum is used for a change of TiN.

[0034] in the above-mentioned example, although BST was used as a high dielectric constant film, this invention is limited to this material -- not having -- a strontium titanate (SrTiO<sub>3</sub>), a barium titanate (BaTiO<sub>3</sub>), and TiO(Pb, Zr) 3 SrBi<sub>2</sub> Ta 2O<sub>9</sub> etc. -- other high dielectric films are sufficient

[0035] Although the DC magnetron-sputtering method was used as the membrane formation method of an electrode and a dielectric in the above-mentioned example, this invention may not be limited to this but the RF magnetron-sputtering method, an efficient consumer response spatter, and \*\*\*\*\* are sufficient as it.

[0036] Although Ru was used in the above-mentioned example, this invention may not be limited to this material, but RuO<sub>2</sub> is sufficient as it.

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[Translation done.]

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] It is the cross section of the thin film capacitor in which one example of this invention is shown.

[Drawing 2] Drawing 2 (a) - (c) is the manufacturing process view of the thin film capacitor in which one example of this invention is shown.

[Drawing 3] Drawing 3 (a) - (c) is the manufacturing process view of the thin film capacitor in which one example of this invention is shown.

[Description of Notations]

1 Up Electrode

2 High Dielectric Constant Film

3 Lower Electrode

4 SiO<sub>2</sub>

5 Si Substrate

6 1st Electrode Layer

7 2nd Electrode Layer

8 Resist

9 Ru

10 TiN

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[Translation done.]

**\* NOTICES \***

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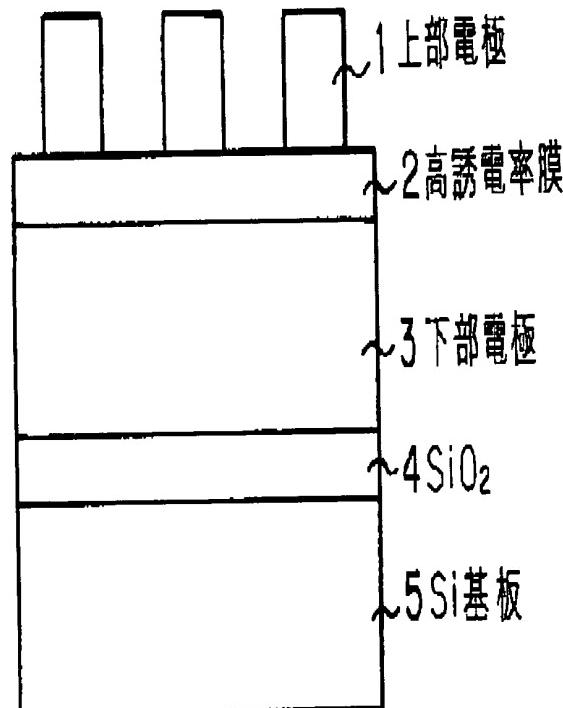
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(54)【発明の名称】 薄膜キャパシタ、その製造方法および電極の加工方法

(57)【要約】

【課題】 リーク電流密度が小さく、電気的特性の優れた薄膜キャパシタ、その製造方法及び電極の加工方法を提供する。

【解決手段】 高誘電率薄膜2が下部電極膜3及び単層または複数層からなる上部電極膜1で挟まれた構造の薄膜キャパシタであって、上部電極1の少なくとも高誘電率膜2に接する電極層がRu或はRuO<sub>2</sub>であり、前記電極層の膜厚が50nm未満であることを特徴とする。



## 【特許請求の範囲】

【請求項1】 高誘電率薄膜が、下部電極膜、及び単層或は複数層からなる上部電極膜で挟まれた構造の薄膜キャパシタにおいて、該上部電極膜の少なくとも該高誘電率膜に接する第1の電極層がルテニウム(Ru)、或は酸化ルテニウム(RuO<sub>2</sub>)であり、かつ前記電極層の膜厚が50nm未満であることを特徴とする薄膜キャパシタ。

【請求項2】 高誘電率薄膜が、下部電極膜、及び単層或は複数層からなる上部電極膜で挟まれた構造の薄膜キャパシタの製造方法において、該上部電極薄膜の少なくとも該高誘電率膜に接する電極層としてルテニウム(Ru)、或は酸化ルテニウム(RuO<sub>2</sub>)を形成する工程と、該上部電極薄膜の最上層である第2の電極層として、酸素を含む雰囲気でのドライエッチングによりエッチングされないか、或はドライエッチングのエッチング速度が第1の電極層のエッチング速度の1/10以下である導電性電極材料を形成する工程を少なくとも含むことを特徴とする薄膜キャパシタの製造方法。

【請求項3】 前記第2の電極層はアルミニウム(AI)、チタン(Ti)、或は窒化チタン(TiN)のいずれかである請求項2記載の薄膜キャパシタの製造方法。

【請求項4】 高誘電率膜が、下部電極、及び上部電極で挟まれた構造の薄膜キャパシタの製造方法であり、少なくとも下部電極、或は上部電極にルテニウム(Ru)、或は酸化ルテニウム(RuO<sub>2</sub>)層の酸素を含む雰囲気でのドライエッチングの工程が含まれる製造方法において、該ルテニウム、或は酸化ルテニウムの電極層をドライエッチの工程が、該電極の最表面がアルミニウム(AI)、チタン(Ti)、或は窒化チタン(TiN)のいずれかで形成された電極構造でのエッチング工程であることを特徴とする薄膜キャパシタの製造方法。

【請求項5】 単層、或は複数層で構成された電極で、かつ前記電極にルテニウム(Ru)、或は酸化ルテニウム(RuO<sub>2</sub>)の層が含まれ、かつ該ルテニウム(Ru)、或は該酸化ルテニウム(RuO<sub>2</sub>)が酸素を含む雰囲気でのドライエッチング工程を有する電極の加工方法において、前記ドライエッチングの工程が、該電極の最表面がアルミニウム(AI)、チタン(Ti)、或は窒化チタン(TiN)のいずれかで形成された電極構造でのエッチング工程であることを特徴とする電極の加工方法。

## 【発明の詳細な説明】

## 【0001】

【発明の属する技術分野】 本発明は、薄膜キャパシタ、その製造方法および電極の加工方法に関し、特に半導体装置用、集積回路用の薄膜キャパシタに関するものである。

## 【0002】

【従来の技術】 1Gbbit以上の次世代高密度DRAM用容量膜に適用するために、誘電特性、絶縁性、化学的安定性に優れたSrTiO<sub>3</sub>、(Ba, Sr)TiO<sub>3</sub>(以下、BSTという)、(Pb, Zr)TiO<sub>3</sub>等のペロブスカイト型酸化物誘電体薄膜の研究開発が行われている。同時に、誘電体薄膜の電気特性はその電極材料やプロセスに強く依存するため、電極材料の検討も重要である。

【0003】 Ru、或はRuO<sub>2</sub>はその加工性が良好であるという特徴を有し、BST膜の電極材料としての適用が検討されている。電極材料としてRuを用いた薄膜キャパシタおよびその製造方法については、インターナショナル・エレクトロン・デバイス・ミーティング『IEDM』“1995年、テクニカルダイジェスト、115～118頁、及び同テクニカルダイジェスト、903～906頁に、それぞれA.ユウキ等、及びY.ニシオカ等によって詳細に報告されている。

【0004】 従来の高誘電率膜としてチタン酸バリウムストロンチウム((Ba, Sr)TiO<sub>3</sub>; 以下BSTと略す)を用い、上部電極がRu単層を用いた薄膜キャパシタには、Ruの膜厚の記載はない。また、従来の薄膜キャパシタの製造方法では、Ruの微細加工は、SiO<sub>2</sub>マスクを用いて反応性イオンエッチング法により行われている。

## 【0005】

【発明が解決しようとする課題】 一般に、薄膜キャパシタの容量を増加させるためには、電極間隔、つまり容量膜である高誘電率膜の膜厚を薄くすることが必要である。特に、1Gbbit以上の次世代高密度DRAMを考えた場合においてはBSTなどの高誘電率膜を用いても20～30nm程度の極薄膜化が必要である。しかしながら、このような高誘電率膜の極薄膜化は薄膜キャパシタのリーク電流を増大させるという問題がある。一般に、キャパシタの面積を勘案し、このような薄膜キャパシタのリーク電流密度は、1V印加時で $1 \times 10^{-8} A/cm^2$ 以下が必要とされている。

【0006】 従来の薄膜キャパシタにおいては、BSTの膜厚が25nmであるとき、1V印加時でのリーク電流密度は約 $4 \times 10^{-8} A/cm^2$ であり、要求される電流密度に達していないという問題があった。

【0007】 他方、従来の薄膜キャパシタの製造方法では上部電極Ruの加工の際、Ru電極の上にSiO<sub>2</sub>を成膜し、レジストを塗布して一般的に用いられるフォトリソグラフィ技術によりレジストを加工し、SiO<sub>2</sub>をパターニングして、Ruの加工を行っていた。このように、従来の技術では、SiO<sub>2</sub>の成膜と除去という工程が入りスループットの点で問題があった。

【0008】 また、Ruを1Gbbit以上の次世代高密度DRAMの下部電極に用いる際、Ruを0.1～0.2ミクロンサイズで加工しなければならないが、SiO

2マスクを用いた場合には、上記の理由でスループットの点で問題があると同時に、加工形状に問題があった。これは、 $\text{SiO}_2$ が非晶質であり、Ruドライエッティングに $\text{SiO}_2$ の肩がエッティングされることによって、 $\text{SiO}_2$ マスク面積が小さくなり、加工されたRuが垂直に加工しにくいためである。

【0009】本発明の目的は、リーク電流密度が小さい薄膜キャパシタを提供することにある。また、スループットが高く、低温でのプロセスであるため半導体の回路特性を劣化させることがない薄膜キャパシタの製造方法を提供することにあり、更に、超高密度集積回路の加工が目的の加工形状で達成できる薄膜キャパシタの製造方法及び電極の加工方法を提供することにある。

#### 【0010】

【課題を解決するための手段】前記の目的は以下の手段によって達成される。すなわち、本発明は、高誘電率薄膜が、下部電極膜、及び単層或は複数層からなる上部電極膜で挟まれた構造の薄膜キャパシタにおいて、該上部電極膜の少なくとも該高誘電率膜に接する第1の電極層がルテニウム(Ru)、或は酸化ルテニウム( $\text{RuO}_2$ )であり、かつ前記電極層の膜厚が50nm未満であることを特徴とする薄膜キャパシタを提案するものである。

【0011】また、本発明は、高誘電率薄膜が、下部電極膜、及び単層或は複数層からなる上部電極膜で挟まれた構造の薄膜キャパシタの製造方法において、該上部電極薄膜の少なくとも該高誘電率膜に接する電極層としてルテニウム(Ru)、或は酸化ルテニウム( $\text{RuO}_2$ )を形成する工程と、該上部電極薄膜の最上層である第2の電極層として、酸素を含む雰囲気でのドライエッティングによりエッティングされないか、或はドライエッティングのエッティング速度が第1の電極層のエッティング速度の1/10以下である導電性電極材料を形成する工程を少なくとも含むことを特徴とする薄膜キャパシタの製造方法を提案するものであり、前記第2の電極層はアルミニウム(AI)、チタン(Ti)、或は窒化チタン(TiN)のいずれかであることを含む。

【0012】また、本発明は、高誘電率膜が、下部電極、及び上部電極で挟まれた構造の薄膜キャパシタの製造方法であり、少なくとも下部電極、或は上部電極にルテニウム(Ru)、或は酸化ルテニウム( $\text{RuO}_2$ )層の酸素を含む雰囲気でのドライエッティングの工程が含まれる製造方法において、該ルテニウム、或は酸化ルテニウムの電極層をドライエッチの工程が、該電極の最表面がアルミニウム(AI)、チタン(Ti)、或は窒化チタン(TiN)のいずれかで形成された電極構造でのエッティング工程であることを特徴とする薄膜キャパシタの製造方法を提案するものであり、更に本発明は単層或は複数層で構成された電極で、かつ前記電極にルテニウム(Ru)、或は酸化ルテニウム( $\text{RuO}_2$ )の層が含ま

れ、かつ該ルテニウム(Ru)、或は該酸化ルテニウム( $\text{RuO}_2$ )が酸素を含む雰囲気でのドライエッティング工程を有する電極の加工方法において、前記ドライエッティングの工程が、該電極の最表面がアルミニウム(AI)、チタン(Ti)、或は窒化チタン(TiN)のいずれかで形成された電極構造でのエッティング工程であることを特徴とする電極の加工方法を提案するものである。

#### 【0013】

【発明の実施の形態】以下、本発明を更に詳細に説明する。

【0014】本発明者等は、高誘電率膜としてBSTを用い、上部電極としてRu、及び $\text{RuO}_2$ をそれぞれ用いて薄膜キャパシタを形成し、そのリーク電流特性を調べた。下部電極は白金(Pt)である。その結果、上部電極の膜厚を100nm以下にすることによって、リーク電流が減少することを見出した。同時に、膜厚が50nm未満でリーク電流の減少傾向が顕著であることを見出した。上部電極の膜厚が200nmを基準とすると、膜厚が50nmで約1/10に減少し、膜厚が30nmでは約1/15に減少した。この理由の詳細は不明であるが、上部電極形成時のBST膜へのダメージの減少、ストレスの減少が考えられる。

【0015】本発明者等は、高誘電率膜としてBSTを用い、BSTに接する上部電極層としてRu、 $\text{RuO}_2$ の上部にAI、Ti及びTiNをそれぞれ形成した。この上にレジストを塗布し、通常のフォトリソグラフィ技術によりレジストを加工し、それをマスクとしてRu、 $\text{RuO}_2$ の上のそれぞれの導電性電極をドライエッティングした。この時、塩素ガスを用いた。続けて、酸素を含む雰囲気でRu、 $\text{RuO}_2$ をドライエッティングすると、Ru、 $\text{RuO}_2$ のエッティングとともにレジストもエッティングが進行するが、Ru、 $\text{RuO}_2$ の上の導電性電極はエッティングさせず、Ru、 $\text{RuO}_2$ を加工することができることが分かった。残存したレジストは $\text{O}_2$ アッシングで容易に除去できた。同時に、Ru、 $\text{RuO}_2$ の上の導電性電極はこのまま上部電極として使用可能であり、不要ならばレジスト除去後連続してドライエッチ可能であることも確認した。この手法では、 $\text{SiO}_2$ の形成、及び除去の工程は必要なく、非常に簡便でスループットが高いことが明らかとなった。また第2の電極層としてドライエッティングのエッティング速度が第1の電極層のエッティング速度の1/10以下の電極材料を用いるようにしても第2の電極をエッティングさせることなく、第1電極のRu、 $\text{RuO}_2$ を加工することができることが分かった。

【0016】同様に、特にRu、 $\text{RuO}_2$ を超微細に加工する際、Ru、 $\text{RuO}_2$ 電極の上面にAI、Ti或いはTiNを形成し、上記と同様な工程でドライエッティング加工を行ったが、AI、Ti或いはTiNはまったく

肩崩れせず、Ru、RuO<sub>2</sub>をほぼ垂直に加工することが可能であった。

【0017】更に、本発明を図面を参照して説明する。

【0018】図1は本発明の薄膜キャパシタの一例を示す断面図である。本発明の薄膜キャパシタは図1に示すように、基板表面が熱酸化で形成されたSiO<sub>2</sub>4を有するシリコン(Si)基板5上に高誘電率薄膜2が下部電極3及び上部電極膜1で挟まれた構造を設けてなるものである。

【0019】高誘電率薄膜2としてはSrTiO<sub>3</sub>、(Ba, Sr)TiO<sub>3</sub>(BST)、BaTiO<sub>3</sub>、(Pb, Zr)TiO<sub>3</sub>、SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub>等が挙げられ、厚みは15~200nmの範囲が好ましい。

【0020】上部電極膜1は単層或は複数層からなり、少なくとも高誘電率膜に接する第1の電極層はルテニウム(Ru)、或は酸化ルテニウム(RuO<sub>2</sub>)からなり、かつその膜厚が50nm未満5nm以上であることが特に肝要である。

【0021】膜厚が50nmを越えると薄膜キャパシタのリーク電流を増大させるので好ましくなく、5nm未満では均一膜が得られにくい(面内での局所的不連続の)問題があり好ましくない。また上部電極膜1が複数層からなる場合は第2の電極膜としては、アルミニウム(AI)、チタン(Ti)或は窒化チタン(TiN)が好ましく用いられる。

【0022】また下部電極3としてPt、Ru、RuO<sub>2</sub>、Ir、IrO<sub>2</sub>等が挙げられ、厚みは5~500nmの範囲が好ましい。

【0023】前記の膜はいずれもDCマグネトロンスパッタ法、RFマグネットロニスパッタ法、ECRスパッタ法、気相成長法等の方法で成膜可能である。

【0024】

【実施例】以下本発明を実施例により更に具体的に説明する。

【0025】(実施例1)以下、本発明の実施例について、図1を参照しながら説明する。図1は実施例1に関わる薄膜キャパシタの断面図である。高誘電率膜2としてBSTを用い、基板表面が熱酸化で形成されたSiO<sub>2</sub>4を有するシリコン(Si)基板5上に、下部電極3としてPt、高誘電率膜2、上部電極として単層のRuが30nm形成された構造となっている。この実施例では、BST膜厚は30nmであり、すべての膜はDCマグネトロンスパッタリング法によって形成した。上部電極の形状は、0.2mmφの円形である。電気特性を測定した結果、誘電率は、290であり、リーク電流密度Jは $8 \times 10^{-9} \text{ A cm}^{-2}$ であった。本発明のRuの薄膜化の効果を調べるために、同じ試料に対し上部電極であるRuの膜厚を200nmまで変化させて調べた結果、200nmでJは $8 \times 10^{-8} \text{ A cm}^{-2}$ 、100nmで $1.5 \times 10^{-8} \text{ A cm}^{-2}$ であり、本発明の効果が確認され

た。誘電率は、上部電極の膜厚によらず一定であった。

【0026】(実施例2)実施例1と同様に、高誘電率膜2としてBSTを用い、基板表面が熱酸化で形成されたSiO<sub>2</sub>4を有するシリコン(Si)基板5上に、下部電極3としてPt、高誘電率膜2、上部電極としてRu(30nm)、AI(100nm)が下から順に積層された電極である構造となっている。この実施例では、BST膜厚は30nmであり、すべての膜はDCマグネトロンスパッタリング法によって形成した。上部電極の形状は、0.2mmφの円形である。電気特性を測定した結果、誘電率は、290であり、リーク電流密度Jは $8 \times 10^{-9} \text{ A cm}^{-2}$ であった。本発明の効果を調べるために、実施例1で行ったことと同様に、上部電極層のAIの膜厚を一定として、Ruの薄膜化の効果を調べた。結果は、実施例1とまったく同一であり、本発明の効果が確認された。

【0027】(実施例3)本実施例では、下部電極3としてRuO<sub>2</sub>、高誘電率膜2としてBST、上部電極1の第1の電極層としてRu、第2の電極層としてTiNを用いた例について、図2を参照しながら説明する。

【0028】基板表面が熱酸化で形成されたSiO<sub>2</sub>4を有するシリコン(Si)基板5上に、下部電極3(RuO<sub>2</sub>)、高誘電率膜2(BST)、上部電極1の第1の電極層6(Ru)、第2の電極層7(TiN)を順次DCマグネトロンスパッタ法で成膜した。膜厚は、下部電極が200nm、BSTは30nm、第1の電極層が30nm、第2の電極層が70nmとした。続けて、レジスト8を塗布し、図2(a)に示す基板を得た。レジストを通常のi線によるリソグラフィ技術により露光、加工し、図2(b)を形成した。この基板をドライエッティング装置に入れ、まず、第2の電極層7であるTiNをCl<sub>2</sub>プラズマガスによりエッティングした。この時、エッティング装置のチャンバ圧力は15mTorr、プラズマパワーは50Wであった。続けて、第1の電極層6であるRuをO<sub>2</sub>とCl<sub>2</sub>の混合ガス(Cl<sub>2</sub>が10%)を用いてエッティングした。この時のチャンバ圧力は20mTorr、プラズマパワーは100Wである。Ruをドライエッティング中にレジストはほとんど消失したが、残存したレジストを除去するため、酸素プラズマによるアッシングにより除去した。その結果、図2(c)に示すような上部電極が加工された薄膜キャパシタが得られた。同様に、第2の電極層として、AI、或はTiを用いて同様な製造方法で検討したが、まったく同様な薄膜キャパシタが得られた。このキャパシタの電気特性は、実施例1、2と同様な良好な特性を示した。

【0029】この工程では、マスクとしてSiO<sub>2</sub>を形成しておらず、本発明の効果が確認された。

【0030】上記実施例では、第2の電極層を除去せず、電極としてそのまま使用したが、レジストをアッシング除去した後、Cl<sub>2</sub>のプラズマガスによるドライエ

ツチングにより第2の電極層7(TiN)を除去した薄膜キャパシタも制作したが、除去しない場合と電気的特性は同一であった。

【0031】(実施例4) 本実施例では、下部電極であるRuを極微細加工した例について図3を用いて説明する。

【0032】基板表面が熱酸化で形成されたSiO<sub>2</sub>4を有するシリコン(Si)基板5上に、Ru9を300nm、TiN10を100nm、DCマグネットロンスパッタ法により成膜した。この基板に化学增幅レジスト8を塗布し、図3(a)なる基板を形成した。電子ビーム露光により、加工寸法0.2ミクロン×0.5ミクロンのパターンを形成し、レジスト8を加工し、図3(b)なる基板を形成した。この基板をドライエッティング装置に入れ、レジスト8をマスクとして、TiN10をCl<sub>2</sub>プラズマによるエッティングを行った。この時のエッティング装置の圧力は15mTorr、プラズマパワーは50Wである。続けて、Ru9をO<sub>2</sub>とCl<sub>2</sub>の混合ガス(Cl<sub>2</sub>が10%)を用いてエッティングした。この時のチャンバ圧力は20mTorr、プラズマパワーは100Wである。Ruをドライエッティング中にレジストは消失した。続けて、TiN10をCl<sub>2</sub>プラズマエッティングし除去し、図3(c)に示す基板を得た。この時のエッティング装置の圧力は15mTorr、プラズマパワーは50Wである。

【0033】得られた基板を電子顕微鏡で観察した結果、設計寸法通りに加工がなされていることを確認した。また、TiNの変わりにTi、或はAlを用いた場合についても実験を行ったが、同一の結果を得た。

【0034】上記実施例では、高誘電率膜としてBSTを用いたが、本発明はこの材料に限定されずチタン酸ストロンチウム(SrTiO<sub>3</sub>)、チタン酸バリウム(BaTiO<sub>3</sub>)、(Pb, Zr)TiO<sub>3</sub>やSrBi<sub>2</sub>TiO<sub>6</sub>など他の高誘電体膜でも良い。

【0035】上記実施例では、電極及び誘電体の成膜方法としてDCマグネットロンスパッタ法を用いたが、本発明はこれに限定されず、RFマグネットロンスパッタ法、ECRスパッタ法、や気相成長法でも良い。

【0036】上記実施例では、Ruを用いたが、本発明はこの材料に限定されず、RuO<sub>2</sub>でも良い。

【0037】

【発明の効果】以上、説明したように、本発明の薄膜キャパシタによれば、リーク電流密度が小さく、電気的特性に優れるという効果がある。また、本発明の薄膜キャパシタの製造方法によれば、スループットが高く、低温でのプロセスであるため半導体の回路特性を劣化させることがない、更に、超高密度集積回路の加工が目的の加工形状で達成できるという効果がある。

#### 【図面の簡単な説明】

【図1】本発明の一実施例を示す薄膜キャパシタの断面図である。

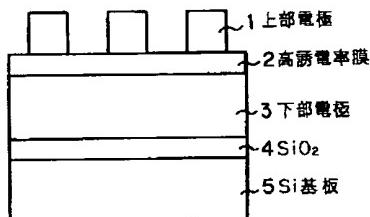
【図2】図2(a)～(c)は本発明の一実施例を示す薄膜キャパシタの製造工程図である。

【図3】図3(a)～(c)は本発明の一実施例を示す薄膜キャパシタの製造工程図である。

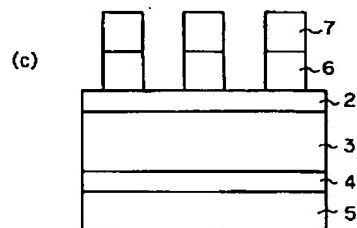
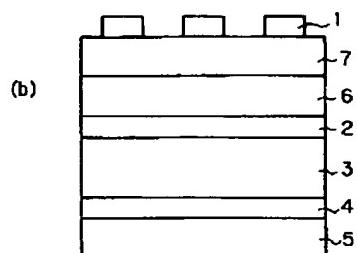
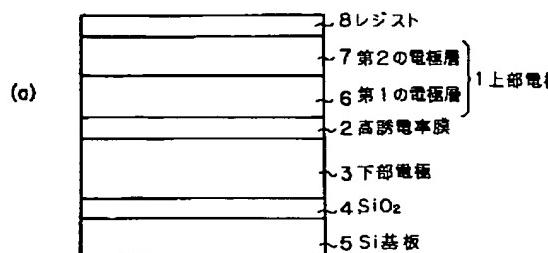
#### 【符号の説明】

- |    |                  |
|----|------------------|
| 1  | 上部電極             |
| 2  | 高誘電率膜            |
| 3  | 下部電極             |
| 4  | SiO <sub>2</sub> |
| 5  | Si基板             |
| 6  | 第1の電極層           |
| 7  | 第2の電極層           |
| 8  | レジスト             |
| 9  | Ru               |
| 10 | TiN              |

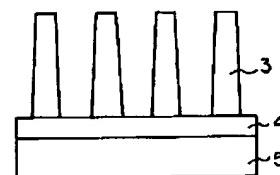
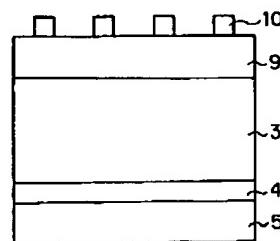
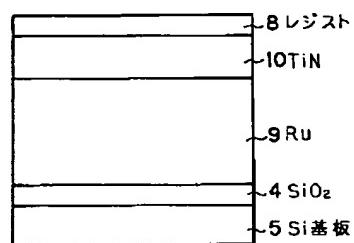
【図1】



【図 2】



【図 3】




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フロントページの続き

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